

CLAIMS

1 1. A method for testing a unit comprising:
2 receiving at least one compressed test vector by the unit;
3 decompressing at least one compressed test vector; and
4 generating at least one output from the unit based at least in part on the testing of the unit
5 with the decompressed test vector.

1 2. The method of claim 1 further comprising:
2 compressing at least one output by the unit; and
3 forwarding the compressed output to a test platform.

1 3. The method of claim 1 wherein decompressing at least one compressed test vector
2 comprises bypassing the decompression if the test vector does not efficiently compress.

1 4. The method of claim 2 wherein compressing at least one output comprises bypassing the
2 compression if the output does not efficiently compress.

1 5. The method of claim 1 wherein the test vector is either one of a functional vectors,
2 parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors, and reset
3 vectors.

1 6. The method of claim 1 wherein receiving at least one compressed test vector comprises
2 loading the compressed test vector with either a single pin of the unit in a serial manner or a
3 plurality of pins in a parallel manner.

1 7. The method of claim 1 wherein the unit is either one of a system on a chip (SoC), an
2 integrated device, or a chipset.

1 8. The method of claim 1 wherein the test platform is either one of a workstation, automatic test
2 equipment, network analyzer, and a logic analyzer.

1 9. A system comprising:
2 a vector generation logic to generate a plurality of test vectors; and
3 a device under test, coupled to the vector generation logic, the system
4 to compress at least one of the plurality of test vectors and to decompress the
5 compressed test vectors when applied to the device under test, and to compress at
6 least one of the plurality of outputs generated by the device under test in response
7 to the decompressed test vector or vectors.

1 10. The system of claim 9 further comprising an analysis logic to receive the decompressed
2 plurality of output or outputs.

1 11. The system of claim 9 wherein the plurality of test vectors is either one of a functional
2 vectors, parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors,
3 and reset vectors.

1 12. The system of claim 9 wherein the device under test is either one of a system on a chip
2 (SoC), an integrated device, or a chipset.

1 13. The system of claim 9 wherein the vector generation logic is either one of a workstation,
2 automatic test equipment, network analyzer, and a logic analyzer.

1 14. The system of claim 10 wherein the analysis logic is either one of a workstation,
2 automatic test equipment, network analyzer, oscilloscope, and a logic analyzer.

1 15. An apparatus comprising:
2 an input port to receive at least one compressed test vector;
3 a decompression logic to decompress the compressed test vector; and
4 the apparatus to generate at least one output based at least in part on the decompressed
5 test vector.

1 16. The apparatus of claim 15 wherein the input port is a single pin or a plurality of pins that
2 receive the test vector(s).

1 17. The apparatus of claim 15 wherein the decompression logic supports a delta method
2 decompression protocol.

1 18. The apparatus of claim 15 wherein the apparatus is either one of a system on a chip
2 (SoC), an integrated device, or a chipset.

1 19. The apparatus of claim 15 wherein test vector(s) is either one of a functional vectors,
2 parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors, and reset
3 vectors.

1 20. The apparatus of claim 15 wherein the apparatus comprises a compression logic to
2 compress the output(s).

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